Greenbank Electronics VDU-KX 1/6/81

Discussion Document. Ref AN-C31/1

CONFIDENTIAL

This document describes a possible design for a new VDU board. It may or may not be produced and it may or may not comply with the description herein. Therefore ..

Please do not tell anybody else about this design, as we do not want to mislead 'normal' customers into thinking this is an imminent new board ~~when~~ as things have not yet reached an advanced stage.

Introduction.

This document describes a single board VDU 203 x 114 mm with a single 43 way connector to be ISBUS-L compatible (but probably gold will be provided on the B-side as well)

The VDU is designed for the sole purpose of replacing the Kemitron VDU-A, B, G set which are inevitably going to be discontinued at some stage.

The VDU-K will therefore be suitable for an existing user who wants to upgrade without needing to change his software in any way.

The foregoing virtually defines the VDU-K specification however the temptation to add some 'improvements' has not been totally resisted, but it is possible that these improvements could be made as a 'retro-fit' to existing VDU A, B, G boards so they will not be rendered totally obsolete.

Essential Features Retained.

1. 32 characters, 24 lines
2. ROM based character generator
3. Bit 7 can be used to provide 'reverse video'
4. No initialisation required

Additional Features Added

1. Lower Case and some graphics characters.
2. Alternative option for bit 7, to give extra 128 characters.
3. All characters held in EPROM, can be optionally user-defined

(4) Bus loading reduced to 1 input load each.
(5) 16 bit address bus (no longer needs DCR-6 to provide 'page select')
(6) Can plug in any slot
(7) NMREQ included in decoding for Z80 use.
(8) CPU speed no longer limited to 2 MHz, VDU-K will operate with 4 MHz Z80 and no wait states. (In fact 4MHz operation is beneficial, see next point)
(9) Improved 'snow' reduction arrangements.
(10) Character cell is now 8×10, adjacent cells touch each other.
(11) Interlaced and non interlaced formats can be provided (previous interlaced display gave some 'flicker' on standard persistence domestic TV sets)
(12) Full T.V. synchronising waveform provided, including ½ line 'equalising pulses' and maintainance of line sync during frame sync time. (Previous absence of these caused some 'pulling' of top row of characters and some 'dithery' pictures on a few makes of TV, particularly colour ones)
(13) UM1233 modulator used (needs no setting up like the earlier UM1231)
(14) Schmitt trigger inputs on NMREQ NRDS NWDS lines, (makes eventual need for earth-plane ~~back~~board less urgent)
(15) Crystal oscillator i.c. used (should reduce occasional failure-to-start problems on previous TTL-gate oscillator)
(16) Master clock reduced in frequency from 7 MHz to 6 MHz – gives slightly wider characters, slightly improved definition, but also makes it easier to generate TV sync waveform which is based on ⅓ µs timing
(17) Single board.

Features omitted

① Option of flashing characters omitted.

② Decoding down to 3/4K omitted (1K of RAM is used, and this has been fitted into a 2K space so that users can now use software for a larger format — e.g 64 chars x 16 lines — it won't look any good still, but at least it will stay on the screen.)

③ Standard components for T.V monitor direct connection (i.e not via modulator) — we will reintroduce these if there's space on the p.c.b.

Main Design Features and Comments.

① Main feature is the use of a "Z80A-CPU/2516/74LS174" TV timing pulse generator. (Comments: a proper T.V. timing pulse generator chip is hard to find, probably around the same price, and fails to give out any other useful pulses - e.g. margins, display 'windows' etc. Other points are - very few chips give non-interlaced display, which we want to make the finished picture look nice, and to synthesise a proper T.V. sync waveform with ordinary LSTTL uses up much too much board space. Finally the VDU-K will make a good 'test bed' for other formats e.g. 64 characters or 80 characters - only a new crystal oscillator, divider, (and RAM if needed) are required - the 2516 can simply be reprogrammed).

Four main outputs are V, H, R, S

V	Vertical reset
H	Horizontal enable
R	Counter reset
S	Mixed horizontal & vertical sync.

(Circuit Diagram sheet 1)

The switch to pin 22 of the 2516 can select a different timing program e.g. interlaced instead of non-interlaced.

(2) Circuit Diagram Sheet 2.

The counters are in LS TTL not programmed, as the replacement for the Kemitron VDU A, B, G may be required urgently and so we have to minimise the magnitude of the software task. (There isn't a tremendous difference in chip count anyway – only one or two packs and the price is almost the same)

(3) Circuit Diagram Sheet 3

Schmitt triggers used for buffering control lines – bus is getting increasingly quicker and noisier now so we want to take out the maximum insurance against earth planes being needed on the backboard.

The 'LS221 provides the 'anti-snow' feature. The 'snow' is not simply blanked out as in previous designs (– not very good now we are using black and white characters; to be invisible on a white background the snow shouldn't be blanked, also blanking shouldn't commence, as previously, at the time of the MPU access – it takes a while for wrong addresses and data to ripple through the RAM and character generator and so blanking isn't needed 'til then)

The method used here takes advantage of the small number of characters employed – 32. (This is one benefit of 32 characters)

The time between characters (1333 ns) is sufficient for a Z80A to get a memory read and write in without disturbing the VDU too much, provided the character generator ROM inputs have the correct data safely latched. The signal called $\overline{\text{LATCH}}$ carries this out.

The monostable ('LS221) is used to delay the re-enabling of the latch, after the microprocessor has finished with the Video RAM, to ensure that the data is good.

The microprocessor is busiest in the VDU when it is doing a block move (the instruction most people use for scrolling). The timing at 4 MHz is ... as follows.

The whole job takes 500 + 250 + 500 = 1250 ns and there is only 250ns spare in the middle. For this reason 200ns 2114 memories are needed to give the best chance of 'snow removal'.

Consideration has not been given to the question of actually executing op-codes in the Video RAM. Timing then is extremely stringent, and the technique has little or no practical ~~value~~ applicati (If you want to give yourself an epileptic fit try executing some op-codes stored in the video RAM in ~~Kemston's~~ the VDU-A, -B, -G !)

NMREQ is issued by a Z80-CPU at refresh time, and in certain adverse circumstances the upper address lines might have a video

address. It normally wouldn't matter because neither NRDS nor NWDS coincide with NRFSH and so a false read or write wouldn't occur, but in this circuit the monostable could be fired at NRFSH time. For tidyness' sake NRFSH has been brought into the decoding to prevent this happening (not that it would do any harm - we don't know exactly.)

On the LHS of the sheet 3 is a switch which brings in the combined read/write strobe RWS. The switch is open for Z80 use and closed for SC/MP use (The SC/MP is so slow even at 4 MHz that it would monopolise the VDU so long that snow would be inevitable, unless the switch is closed — then the effective length of time it requires access is reduced to about 500ns, the length of the SC/MP read or write strobe).

Decoding is only for 2K, this means the 1K video RAM will repeat. This is deliberate as software from other systems with larger numbers of characters no longer have them fall off the end of the screen — they wrap round and reappear at the top. Ugly, but at least they're there.

④ Sheet 4

The latch previously described is here, and the familiar 157 multiplexers. The chip selects and buffer direction/enable have been arranged to give a much better 'overlap' than the 2114 requires. The 2114 data gives 0ns for the following parameters, which makes it a dream to use, but the new-fangled

memories may not be so forgiving (We are actively looking at the CMOS 6116 which will be a very useful 2K×8 candidate for a Video RAM etc. when prices drop). 2114 'Ons parameters: —

t_{AW}	address to write setup	Ons.
t_{WR}	write release	Ons
t_{DH}	data hold	Ons

⑤ Circuit Diagram Sheet 5.

Two 2516 character generators are shown. One is the main char. gen (Upper + lower case ASCII etc) the other is 'up for grabs'. S1 in the top left hand corner .. lets reverse video be the result of a '1' on the highest data bit (Bit LD7) — this is essential as an option to suit existing software users particul ZYMON 1 which needs it for its cursor.

(There was a wish to make one of the character generators programmable at run time by using a 6116 2K RAM instead, but this was just too many chips, and certainly is stepping outside the brief of a 'VDU A,B G replacement'.)

A synchronous shift register is used to get 8 absolutel even dots so no 'join' between characters should be noticed, and a 74LS74 has been used to get the display 'enable' window' to fit exactly over 32 characters — no shadowy half dots at the end we hope.

The method used for enabling the display and generating the frame and line syncs is under

the control of the fancy (microprocessor-controlled) timing generator and: it has been arranged that there will never be any video data during sync. time or sync during video time. In consequence the interface to the UM1233 is very simple (which is a relief because we have no spare board space!) and is simply two resistors, values yet to be decided exactly. We are not sure if we should rely on a logic '1' being 3½ volts - nobody will guarantee it more closely than 2½ - 5 volts. We don't yet know if it matters anyway, the UM1233 seems to be very forgiving so far.

Progress

We have built a handwired giant breadboard of the circuit, although not with exactly the same devices or pin numbers so this circuit cannot yet be called tested.

The prototype seems to work O.K. and so any interested readers of this document are invited to build one for themselves if they desire, we will be pleased to supply a suitable timing program ROM and character generator ROM if needed.

Note that a fairly dense layout is needed to fit the 26 ics (etc) on a 203 × 114 mm card — we suggest the use of a simple 'veroboard' pattern card rather than the usual 'breadboard' pattern which only takes around 20 ics.

We are not absolutely certain that we will be able to fit all the circuitry onto a printed circuit board, but we intend to have a jolly good attempt — it will undoubtedly mean through hole plating, but this is not necessarily a bad thing.

The projected cost of the components is surprisingly low due to the following two main factors.

(i) No fancy 'superchip' is used (e.g 6845, Thomson SFF...)
(ii) The Z80A-CPU ·., 2516 and 2114 are all at very much reduced prices at present.

In any event, in comparing prices we must compare like with like — if it doesn't have a proper TV. sync waveform then it isn't a VDU-K!

DMP. 1/6/81

Proposed character set ("main" char. gen. ROM) 128 chars

① Low ASCII numbers (00, 01, 02 etc) - 'Pixel' style graphic characters with binary weighting
e.g  etc.

② ASCII Upper Case } 64 characters (generally as in 'RO-3-2513' standard character generator)
" Punctuation }

③ ASCII Lower Case, with decenders.

④ Characters for Ruling Boxes
e.g ┘ └ ┌ ┐ ┴ ┼ etc.

⑤ Special extra characters.
£ sign.
2 Similar 'robots' (but different enough to provide animation)
2 character 'Space Invader' vehicle.
etc.

Alternative Character Set 128 chars.
128 characters, as yet undefined.

(Note these are only available as an alternative option to that of a 'reverse video' set of the main char. gen ROM characters i.e. both options are not possible - there are only 256 permitted characters in all).

Benefits of 32 × 24 format.

1. Long time between characters (1333ns), makes 'anti-snow' circuitry a possibility, with no wait states or other restrictions on CPU operating speed.

2. Characters are approximately square which makes 'pretty' displays possible.

3. 32 characters ... gives 'big' letters which are easier to read at a distance e.g classroom use.

4. Big size gives better results for some games e.g. the bigger the Space Invaders are the better we like them.

5. Animation is quicker the ~~less~~ fewer character spaces there are to move around.

VDU-KX

Modification made to circuit diagram sheet 3

2-6-81.

NMREQ & NRFSH Gates re-organised so that space is released in the '136 input set for AB10 – decoding is now right down to 1K.

Retriggerable monostable now substituted for earlier ½74LS221 – the duty cycle required was so high when block move was being executed that only retriggerable type can cope. (Pin nos and timing components also altered to suit.)

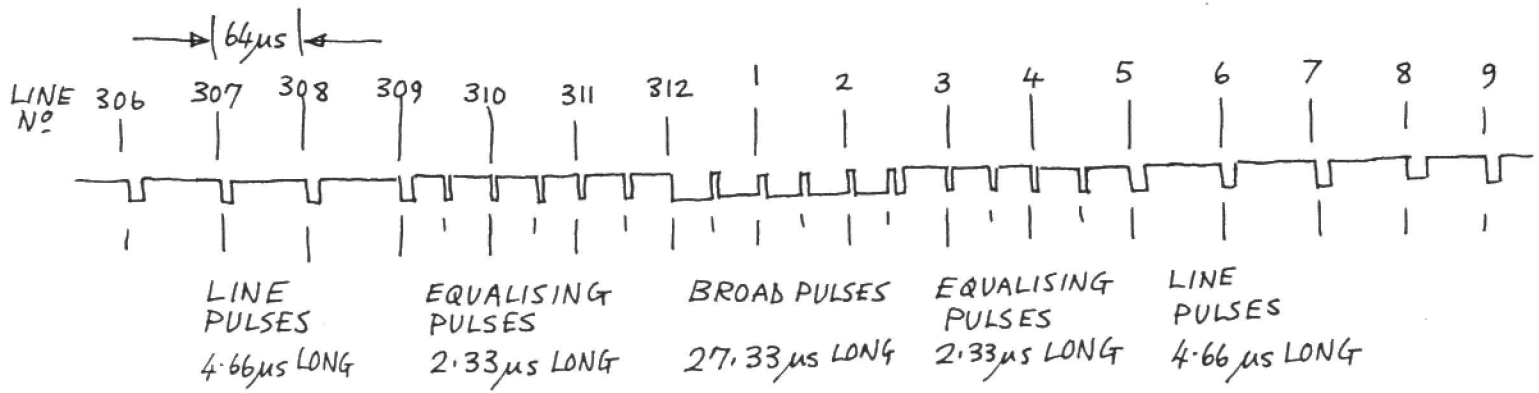
Setting up instructions (e.g. Tiny BASIC V5.Ø1)

```
RUN     1Ø  P.'XXXXXXXXXXX'
        2Ø  G. 1Ø
```

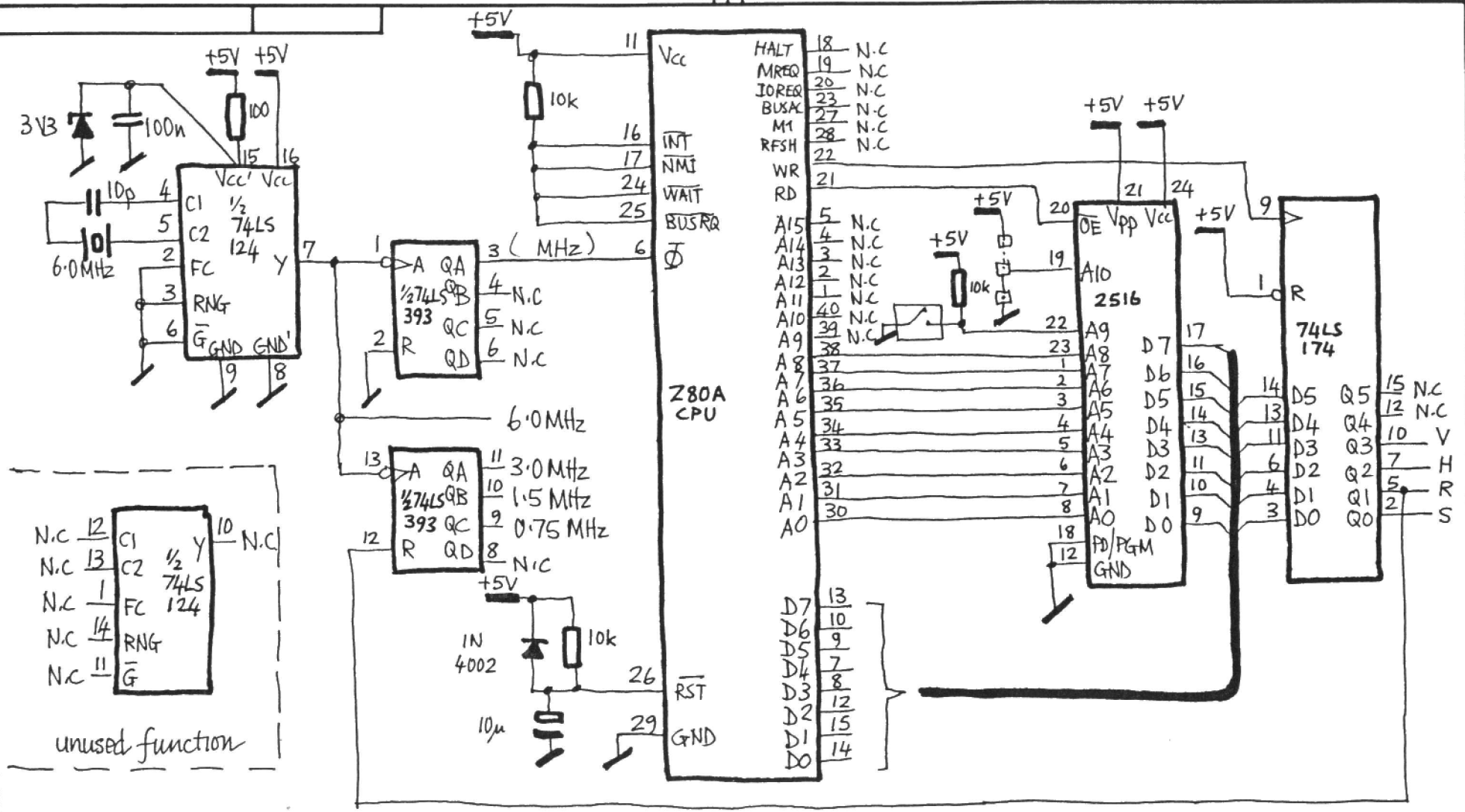
and adjust RV1 for minimum 'snow'. (4MHz Z80 only)

With 200ns 2114's and worst case buffer delays first calculations made indicate execution of op-codes @ 4MHz in video RAM is not possible unless wait states are added to op-code fetch. This restriction accepted – VDU A, B, G wasn't supposed to work at 4MHz anyway. Also executing op-codes in video RAM is just a smartypants trick – no real practical use.

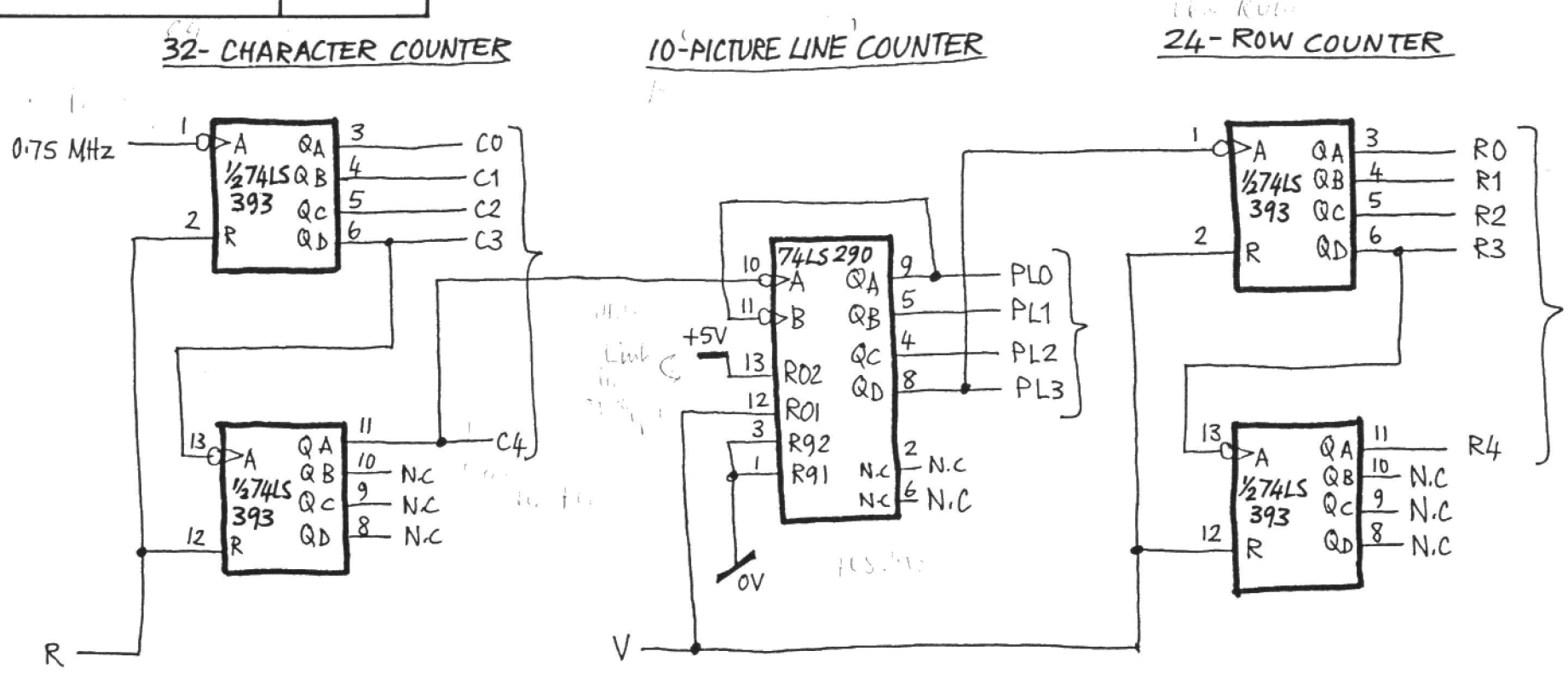
D.M.P 2/6/81



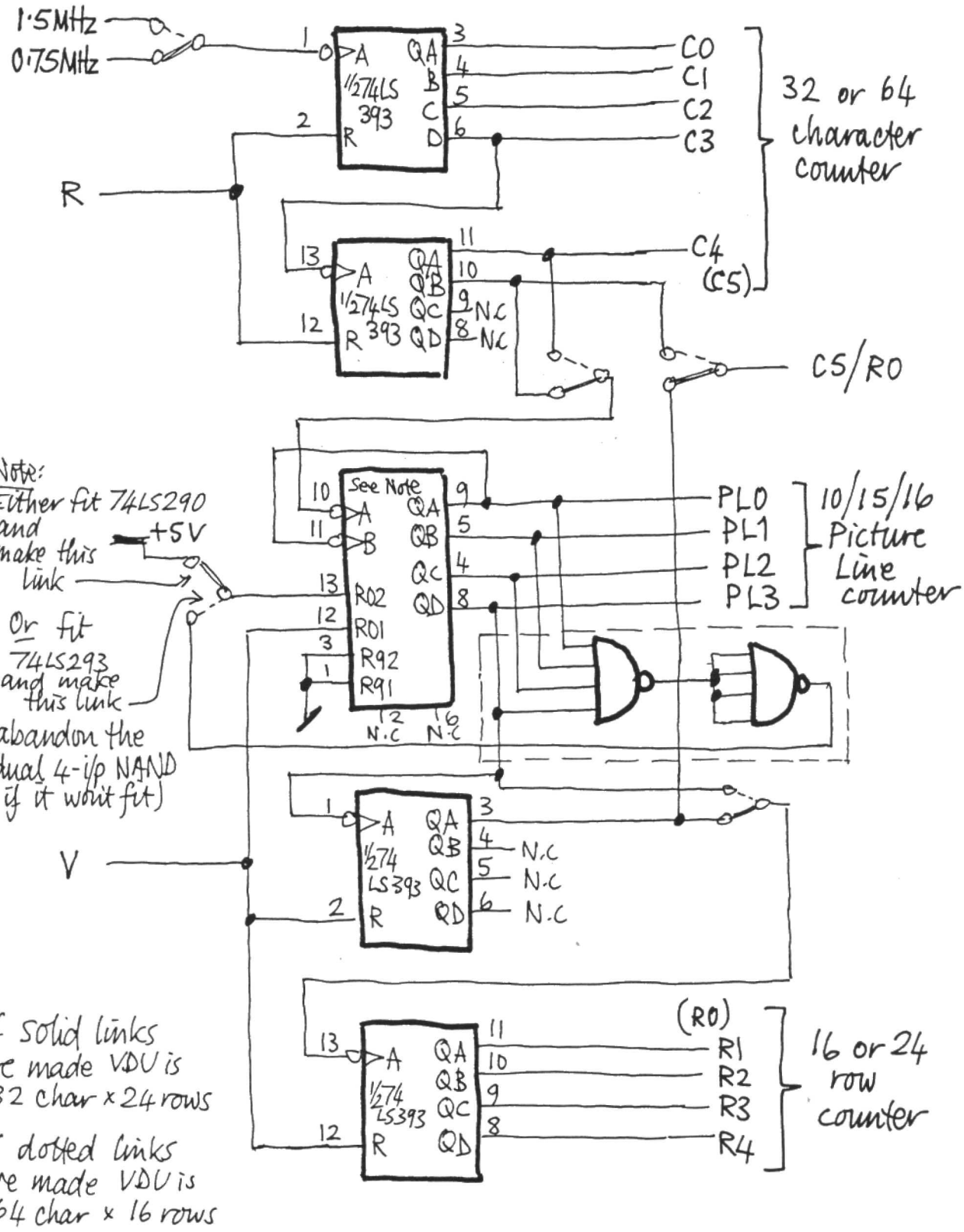
	Drawn DMP	**Greenbank Electronics**
	Date 1-6-81	TELEVISION SYNC. PULSE WAVEFORM REQUIRED
	Scale –	



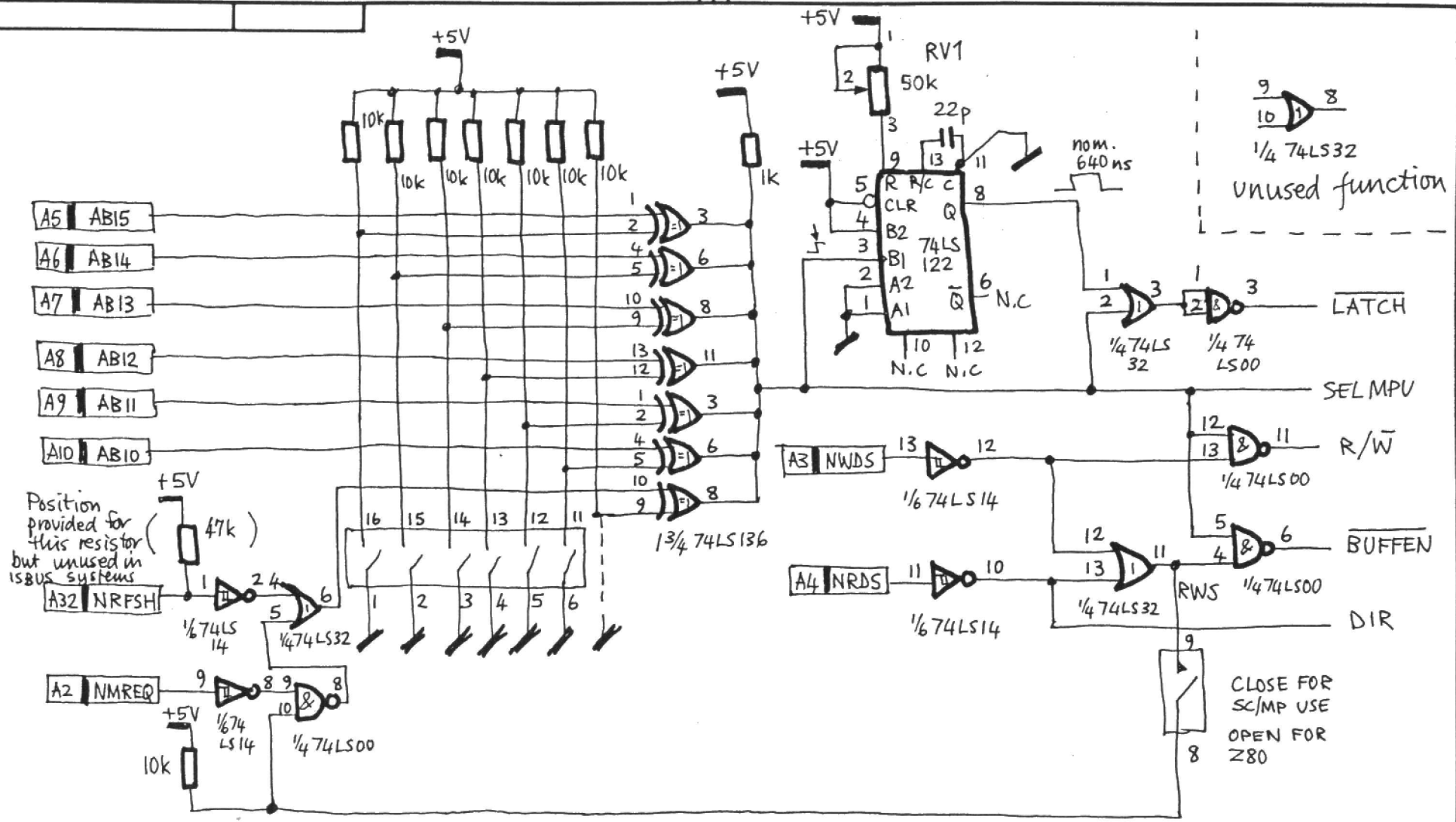
	Drawn D.M.P.	**Greenbank Electronics**
	Date 30-5-81	VDU-KX CIRCUIT DIAGRAM
	Scale ~	SHEET 1 OSCILLATOR AND TIMING
		1



	Drawn D.M.P.	**Greenbank Electronics**
	Date 30-5-81	VDU-KX CIRCUIT DIAGRAM
	Scale -	SHEET 2 CHARACTER ETC. COUNTERS
		2



This drawing replaces sheet 2 of original circuit diagram 30-5-81	Drwn DMP Date 4-6-81 Scale —	**Greenbank Electronics** VDU KX ALTERNATIVE COUNTERS FOR 32/64 FORMATS



Drawn	D.M.P
Date	30-5-81
Scale	–
REVISED	2-6-81

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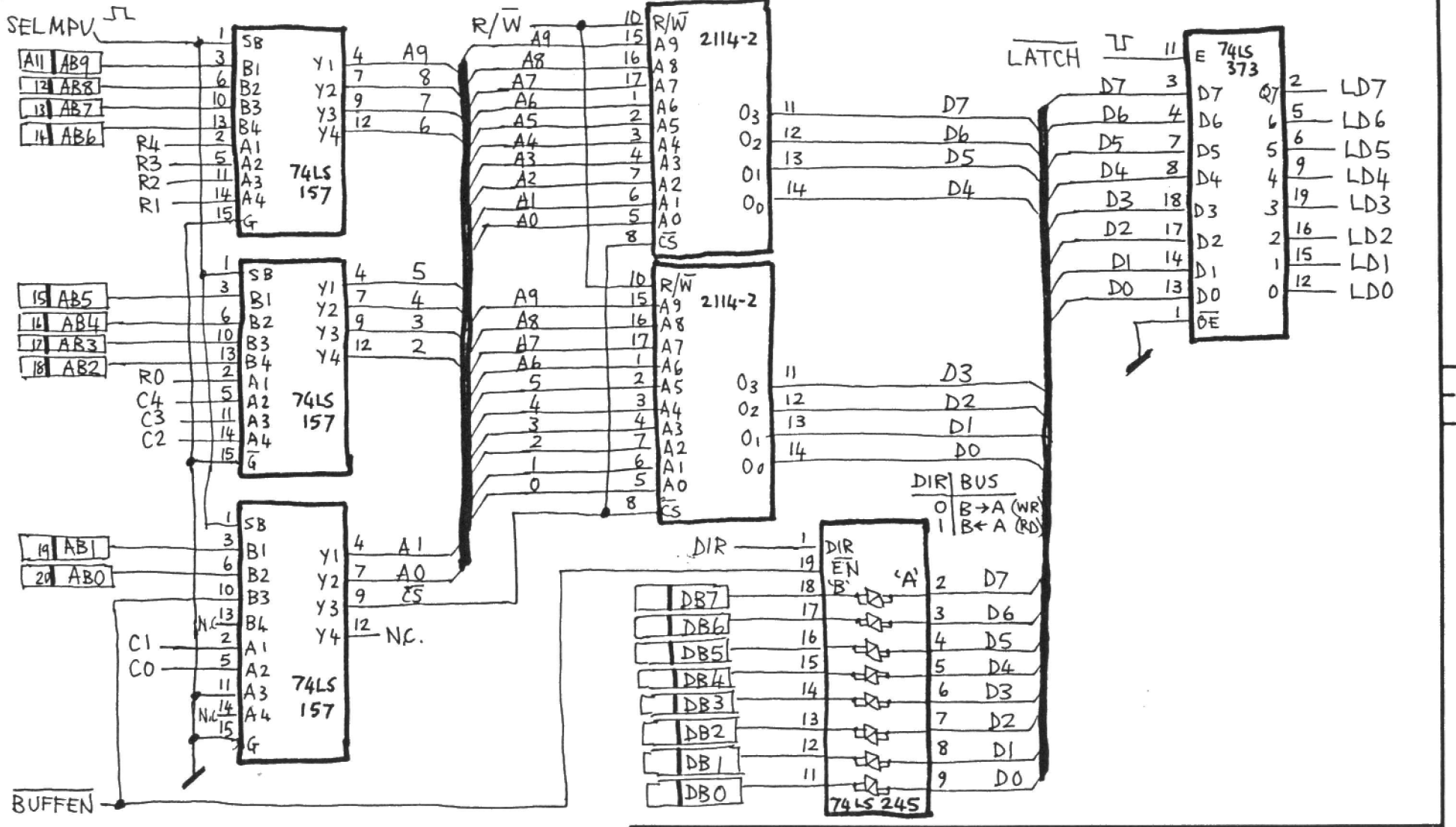
VDU-KX CIRCUIT DIAGRAM

SHEET 3 ADDRESS DECODER

3



Drawn	D. M. P.
Date	30-5-81
Scale	—

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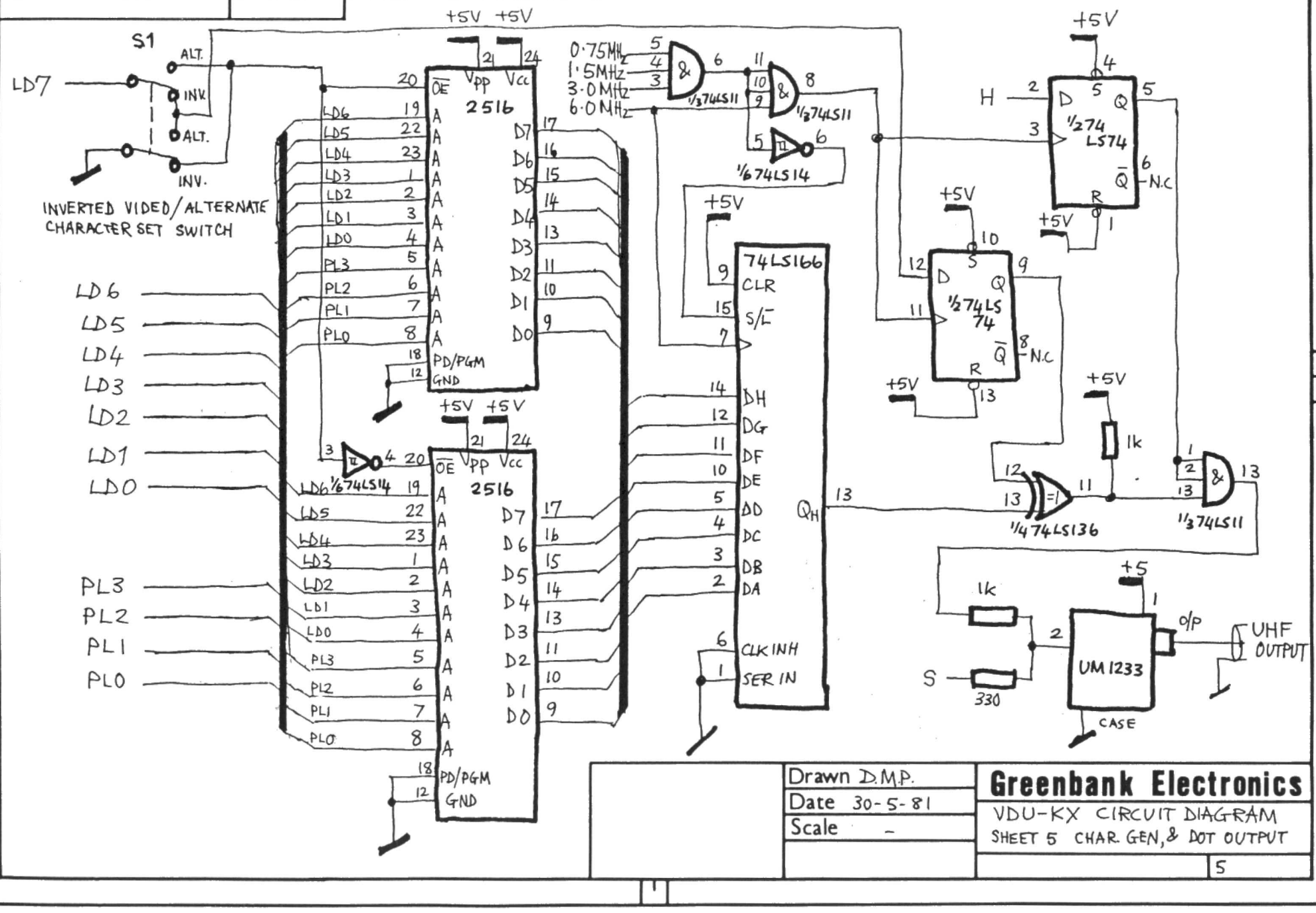
VDU-KX CIRCUIT DIAGRAM

SHEET 4 VIDEO RAM AND MULTIPLEX

4


S1
ALT.
INV.
ALT.
INV.
LD7
INVERTED VIDEO/ALTERNATE CHARACTER SET SWITCH
+5V
2516
OE
Vpp
Vcc
A
D7
D6
D5
D4
D3
D2
D1
D0
PD/PGM
GND
LD6
LD5
LD4
LD3
LD2
LD1
LD0
PL3
PL2
PL1
PL0
0·75MHz
1·5MHz
3·0MHz
6·0MHz
1/374LS11
1/674LS14
74LS166
CLR
S/L
DH
DG
DF
DE
DD
DC
DB
DA
QH
CLK INH
SER IN
H
1/274 LS74
D
Q
R
N.C
1/274LS 74
1/474LS136
1k
330
UM1233
o/p
UHF OUTPUT
CASE
Drawn D.M.P.
Date 30-5-81
Scale –
Greenbank Electronics
VDU-KX CIRCUIT DIAGRAM
SHEET 5 CHAR. GEN, & DOT OUTPUT
5

Parts List VDU - KX

1-6-81

Resistors

1	100R
1	330R
3	1k
1	2k2
2	10k
2	47k
10	

Sil. Resistor Pack

1	8 x 10Ω	(9 pin).

(9pin SIL.)

Variable Resistors

1	10k

Capacitors

1	10p	
1	100p	
?	100n	(numerous, for decoupling)
1	10µ.	
1	22µ - 100µ	

Diodes.

1	IN 4002
1	3V3 Zener.

continued . . .

Parts list Continued

Integrated Circuits.

1	74LS00	14 pin
1	74LS11	14 "
1	74LS14	14 "
1	74LS32	14 "
1	74LS74	14 "
1	74LS124	16 "
2	74LS136	14 "
3	74LS157	16 "
1	74LS166	16 "
1	74LS174	16 "
1	74LS221	16 "
1	74LS245	20 "
1	74LS290	14 "
1	74LS373	20 "
3	74LS393	14 "
2	2114 - 200ns	18 "
3	2516	24 "
1	Z80A - CPU	40 "
26		

Quartz Crystal.

1	6.0 MHz

Misc.

1	16 pin DIL switch pack	16 pin.
1	UM1233 UHF Modulator	
1	DPDT Toggle switch.	
1	UHF Aerial socket.	
1	Front Panel.	

Sockets.

1 x 9 SIL pin, 11 x 14 pin, 8 x 16 pin, 2 x 18 pin, 2 x 20 pin, 3 x 24 pin, 1 x 40 pin